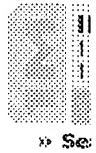


Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	4396	(scan adj2 test\$3)	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:17
L2	87	(scan adj2 test\$3) and edge-triggered	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:18
L3	85	(scan adj2 test\$3) and edge-trigger\$3 and (flip-flop\$1 or latch\$3)	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:18
L4	21	(scan adj2 test\$3) and (edge-trigger\$3 or (edge adj2 trigger\$3)) and (flip-flop\$1 or latch\$3) and (combinatorial adj2 logic)	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:20
L5	16	(scan adj2 test\$3) and (edge-trigger\$3 or (edge adj2 trigger\$3)) and (flip-flop\$1 or latch\$3) and (combinatorial adj2 logic) and (multiplex\$3)	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:20
L6	20	(scan adj2 test\$3) and (edge-trigger\$3 or (edge adj2 trigger\$3)) and (flip-flop\$1 or latch\$3) and (combinatorial adj2 logic) and (multiplex\$3 or select\$3)	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:21
L7	22	(scan adj2 test\$3) and (first adj2 domain\$1) and (second adj2 domain\$1)	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:22
L8	19	(scan adj2 test\$3) and (first adj2 clock adj2 domain\$1) and (second adj2 clock adj2 domain\$1)	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:22
L9	57	(first adj2 clock adj2 domain\$1) and (second adj2 clock adj2 domain\$1) and test\$4	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:23
L10	8	(first adj2 clock adj2 domain\$1) and (second adj2 clock adj2 domain\$1) and test\$4 and (edge-trigger\$4 or (edge adj2 trigger\$4))	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:23
L11	8	(first adj2 clock adj2 domain\$1) and (second adj2 clock adj2 domain\$1) and test\$4 and (edge-trigger\$4 or (edge adj2 trigger\$4)) and (latch\$4 or flip-flop\$1)	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:27

L12	54	(clock adj2 domain\$1) and test\$4 and (edge-trigger\$4 or (edge adj2 trigger\$4)) and (latch\$4 or flip-flop\$1)	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:27
L13	13	(clock adj2 domain\$1) and (scan adj2 test\$4) and (edge-trigger\$4 or (edge adj2 trigger\$4)) and (latch\$4 or flip-flop\$1)	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:28
L14	10	(clock adj2 domain\$1) and (scan adj2 test\$4) and (edge-trigger\$4 or (edge adj2 trigger\$4)) and (latch\$4 or flip-flop\$1) and (select\$4 or multiplex\$4)	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:29
L15	0	(plurality adj3 clock adj2 domain\$1) and (scan adj2 test\$4) and (edge-trigger\$4 or (edge adj2 trigger\$4)) and (latch\$4 or flip-flop\$1) and (select\$4 or multiplex\$4)	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:30
L16	8	(clock adj2 domain\$1) and (scan adj2 test\$4) and (edge-trigger\$4 or (edge adj2 trigger\$4)) and (latch\$4 or flip-flop\$1) and (select\$4 or multiplex\$4) and (test adj2 mode)	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:31
L17	5	(clock adj2 domain\$1) and (scan adj2 test\$4) and (edge-trigger\$4 or (edge adj2 trigger\$4)) and (latch\$4 or flip-flop\$1) and (select\$4 or multiplex\$4) and (test adj2 mode) and TDI and TDO and TCK	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:33
L18	40	(clock adj2 domain\$1) and (latch\$4 or flip-flop\$1) and (select\$4 or multiplex\$4) and (test adj2 mode) and TDI and TDO and TCK	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:34
L19	30	(clock adj2 domains) and (latch\$4 or flip-flop\$1) and (test adj2 mode) and TDI and TDO and TCK	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:35
L20	30	(clock adj2 domains) and (latch\$4 or flip-flop\$1) and (test adj2 mode) and TDI and TDO and TCK	USPAT; EPO; JPO; DERWENT	OR	OFF	2004/11/19 09:36

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 Pages:17 - 25

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**5 Advanced synchronous scan test methodology for multi clock domain ASICs***Schmid, J.; Knablein, J.;*

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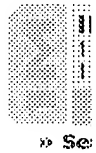
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**10 The testability features of the 3rd generation ColdFire<sup>(R)</sup> family of microprocessors***Crouch, A.L.; Mateja, M.; McLaurin, T.L.; Potter, J.C.; Tran, D.;*

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